CLAIMS

1. A processing system comprises a register file, a switch capable of controlling information pathways and performing routing functions and having a first input coupled to an output of the register file, and an arithmetic logic unit having an input coupled to an output of the switch and an output coupled to an input of the register file.

2. The processing system of claim 1 wherein the switch is a Banyan switch.

3. The processing system of claim 2 wherein the arithmetic logic unit comprises a bitwise function unit with an input coupled to the output of the switch, a pipeline register having an input coupled to an output of the bitwise function unit, and an accumulator having an input coupled to an output of the pipeline register and an output coupled to the input of the register file.

4. The processing system of claim 2 wherein the switch comprises N switching stages, N equal to $\log_M(w)$, w being an internal bitwidth of the switch, and each of the N switching stages having N/2 switching cells.

5. The processing system of claim 4 wherein M is selected from a group comprising 2 and 4.

6. The processing system of claim 2 further comprises a routing unit having a first input coupled to the output of the register file and an output coupled to the first input of the switch.

7. The processing system of claim 5 further comprises a switch control unit having an output coupled to a second input of the switch.

8. The processing system of claim 7 further comprises a constant generator having an output coupled to a second input of the routing unit.

9. The processing system of claim 8 wherein the switch comprises N switching stages, N equal to $\log_M(w)$, w being an internal bitwidth of the switch, and each of the N switching stages having N/2 switching cells.

10. The processing system of claim 9 wherein M is selected from a group comprising 2 and 4.

11. The processing system of claim 9 wherein the routing unit comprises a control logic generating a control signal having groups of bits, and a plurality of logics respectively operating on the groups of bits.

12. The processing system of claim 11 wherein the switch control unit comprises a shift constants generator, a pipeline flip-flop having an input coupled to an output of the shift constants generator, and a switch tree having an input coupled to an output of the pipeline flip-flop.

13. The processing system of claim 2 further comprises a constant generator having an output coupled to the first input of the switch.

14. The processing system of claim 13 further comprises a switch control unit having an output coupled to the first input of the switch.

15. The processing system of claim 2 further comprises a switch control unit having an output coupled to a second input of the switch.

16. A means for processing data comprises a means for reading and writing addresses and data, a means for controlling information pathways and performing routing functions, and a means for performing arithmetic functions and logic functions.

17. The means for processing data of claim 16 wherein the means for performing arithmetic functions and logic functions comprises a means for performing bitwise

functions, a means for performing register functions, and a means for performing additions.

18. The means for processing data of claim 16 wherein the means for controlling information pathways and performing routing functions comprises N means for controlling information pathways and performing routing functions in stages, each of the N means having N/2 means for transferring signals from any input to any output.

19. The means for processing data of claim 16 further comprises a means for selectively aligning and transferring data.

20. The means for processing data of claim 19 further comprises a means for generating control signals that determines particular routing or bitfield manipulation operations.

21. The means for processing data of claim 20 further comprises a means for selectively generating and outputting constants and bitfield mask primitives.

22. The means for processing data of claim 21 wherein the means for controlling information pathways and performing routing functions comprises N means for controlling information pathways and performing routing functions in stages, each of the N means having N/2 means for transferring signals from any input to any output.

23. The means for processing data of claim 22 wherein the means for selectively aligning and transferring data comprises a means for generating a control signal having groups of bits, and a plurality of means for respectively operating on the groups of bits.

24. The means for processing data of claim 23 wherein the means for generating control signals that determine particular routing or bitfield manipulation operations comprises a means for outputting a shift code, a means for performing flip-flop functions, and a means for generating and outputting switch control signals.

25. The means for processing data of claim 16 further comprises a means for selectively generating and outputting constants and bitfield mask primitives.

26. The means for processing data of claim 25 further comprises a means for generating control signals that determine particular routing or bitfield manipulation operations.

27. The means for processing data of claim 16 further comprises a means for generating control signals that determine particular routing or bitfield manipulation operations.

28. A method of processing data comprises reading and writing addresses and data, controlling information pathways and performing routing functions, and performing arithmetic functions and logic functions.

29. The method of processing data of claim 28 wherein the step of performing arithmetic functions and logic functions comprises performing bitwise functions, performing register functions, and performing additions.

30. The method of processing data of claim 28 wherein the step of controlling information pathways and performing routing functions comprises N sub-steps of controlling information pathways and performing routing functions in stages, each of the N sub-steps having N/2 sub-steps of transferring signals from any input to any output.

31. The method of processing data of claim 28 further comprises selectively aligning and transferring data.

32. The method of processing data of claim 31 further comprises generating control signals that determine particular routing or bitfield manipulation operations.

33. The method of processing data of claim 32 further comprises selectively generating and outputting constants and bitfield mask primitives.

34. The method of processing data of claim 33 wherein the step of controlling information pathways and performing routing functions comprises N sub-steps of controlling information pathways and performing routing functions in stages, each of the N sub-steps having N/2 sub-steps of transferring signals from any input to any output.

35. The method of processing data of claim 34 wherein the step of selectively aligning and transferring data comprises generating a control signal having groups of bits, and operating on the groups of bits.

36. The method of processing data of claim 35 wherein the step of generating control signals comprises outputting a shift code, performing flip-flop functions, and generating and outputting switch control signals.

37. The method of processing data of claim 28 further comprises selectively generating and outputting constants and bitfield mask primitives.

38. The method of processing data of claim 37 further comprises generating control signals that determine particular routing or bitfield manipulation operations.

39. The method of processing data of claim 28 further comprises generating control signals that determine particular routing or bitfield manipulation operations.